We Claim:

1. A method for producing a thermoelectric layer structure, which comprises the steps of:

providing a substrate; and

forming at least one electrically anisotropically conductive V-VI layer on the substrate using the aid of one of a seed layer and a structure formed in the substrate, the V-VI layer being formed relative to the substrate with an angle between a direction of highest conductivity of the V-VI layer and the substrate being greater than 0°.

2. The method according to claim 1, which further comprises setting the angle between the direction of the highest conductivity of the V-VI layer and the substrate to be between 30° and 90°.

3. The method according to claim 1, which further comprises forming the seed layer in a textured manner.

4. The method according to claim 1, which further comprises forming the seed layer to have a thickness of less than 500 nm.

5. The method according to claim 1, which further comprises disposing the seed layer in at least two spatially separate regions on the substrate.

6. The method according to claim 1, which further comprises depositing the seed layer electrochemically and disposed one of below and above the V-VI layer.

7. The method according to claim 1, which further comprises forming a vertically structured pattern in a surface of the substrate for forming the structure on the substrate.

8. The method according to claim 7, which further comprises pivoting the substrate by a further angle with respect to the vertical before the vertically structured pattern is formed in the substrate.

9. The method according to claim 8, which further comprises pivoting the substrate by the further angle such that a main deposition direction for the V-VI layer is perpendicular to a starting growth area of the vertically structured pattern.

10. The method according to claim 7, which further comprises:

using a silicon wafer as the substrate; and

etching anisotropically a surface of the silicon wafer to obtain oblique areas for forming the vertically structured pattern.

11. The method according to claim 7, which further comprises depositing an insulating layer on the substrate after a formation of the oblique areas.

12. The method according to claim 1, which further comprises

disposing the V-VI layer on the substrate;

disposing the seed layer above the V-VI layer; and

performing subsequently a heat treatment process, so that the V-VI layer is oriented to produce, proceeding from the seed layer an orientation of the direction of the highest conductivity substantially perpendicular to the substrate.

13. The method according to claim 1, which further comprises applying an electric field for affecting an orientation of the direction of the highest conductivity.

14. The method according to claim 1, which further comprises forming the V-VI layer as a $(Bi, Sb)_2 (Te, Se)_3$ layer.

15. The method according to claim 2, which further comprises setting the angle to be between 85° and 90°.

16. The method according to claim 4, which further comprises setting the thickness to be less than 100 nm.

17. The method according to claim 11, which further comprises using a thermal oxide for forming the insulating layer.

18. The method according to claim 1, which further comprises

disposing the V-VI layer on the substrate;

disposing the seed layer above the V-VI layer; and

performing subsequently a heat treatment process, so that the V-VI layer is oriented to produce, proceeding from the seed layer an orientation of a direction of a lowest conductivity substantially perpendicular to the substrate.

19. A method for producing a thermoelectric layer structure, which comprises the steps of:

providing a substrate; and

forming at least one electrically anisotropically conductive V-VI layer on the substrate with an orientation of the V-VI layer relative to the substrate, being effected by applying an electric field such that an angle between a direction of highest conductivity of the V-VI layer and the substrate being greater than 0°.

20. The method according to claim 19, which further comprises forming the V-VI layer as a $(Bi, Sb)_2 (Te, Se)_3$ layer.

21. The method according to claim 19, which further comprises setting the angle to be approximately 90°.

22. A component, comprising:

a thermoelectric layer structure produced by the method according to claim 1.

23. The component according to claim 22, wherein the component is selected from the group consisting of a Peltier cooler, a thermogenerator, and a thermopile.

24. A component having a thermoelectric layer structure, comprising:

a substrate; and

at least one electrically anisotropically conductive V-VI layer disposed on said substrate, said V-VI layer being disposed such that an angle between a direction of highest conductivity of said V-VI layer and said substrate being greater than 0°.

25. The component according to claim 24, wherein said angle is approximately 90°.

26. The component according to claim 24, wherein said V-VI layer is a $(Bi, Sb)_2 (Te, Se)_3$ layer.